CY7C1051DV33

8-Mbit (512K x 16) Static RAM

Features

- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 110 mA at 10 ns
- Low CMOS standby power
  - I_{SB2} = 20 mA
- 2.0V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 48-ball FBGA and 44-pin TSOP II packages

Functional Description

The CY7C1051DV33[1] is a high performance CMOS Static RAM organized as 512K words by 16 bits.

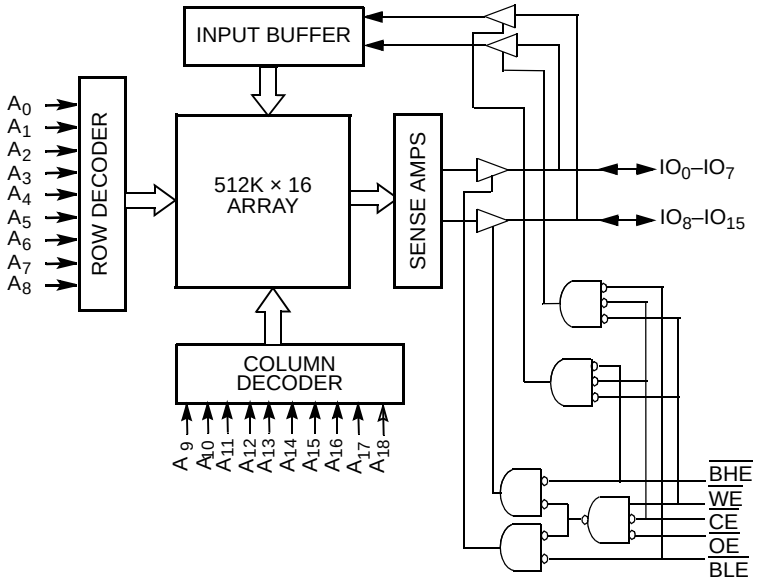
To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0–IO_7), is written into the location specified on the address pins (A_0–A_{18}). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8–IO_{15}) is written into the location specified on the address pins (A_0–A_{18}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appears on IO_0–IO_7. If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the “Truth Table” on page 8 for a complete description of read and write modes.

The input/output pins (IO_0–IO_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), the $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW) is in progress.

The CY7C1051DV33 is available in a 44-pin TSOP II package with center power and ground (revolutionary) pinout and a 48-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram



Note

1. For guidelines about SRAM system design, refer to the Cypress application note AN1064, SRAM System Guidelines available at www.cypress.com.

Pin Configurations

Figure 1. Pin Diagram - Top View 48 Ball mini FBGA[2]

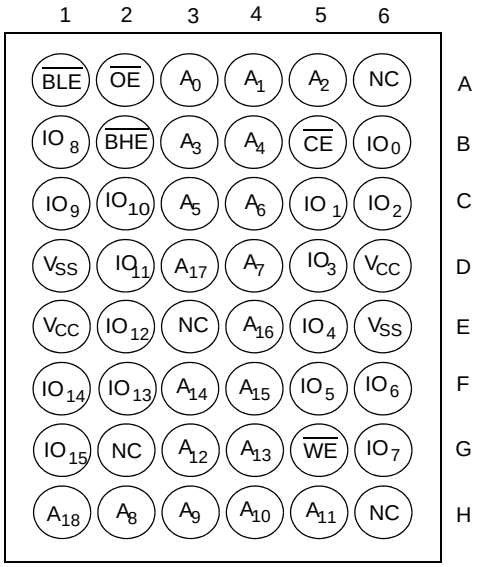
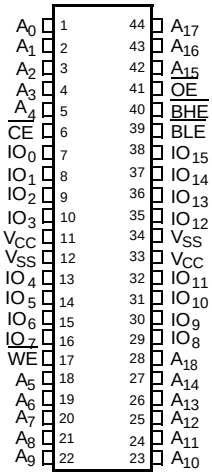


Figure 2. Pin Diagram - Top View TSOP II[2]



Selection Guide

	–10	–12	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	110	100	mA
Maximum CMOS Standby Current	20	20	mA

Note
2. NC pins are not connected on the die

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .....–0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3] ..... –0.3V to V_{CC} + 0.3V

DC Input Voltage[3] ..... –0.3V to V_{CC} + 0.3V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... .....>2001V (per MIL-STD-883, Method 3015)

Latch up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	3.3V ± 0.3V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	–10		–12		Unit
			Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA		0.4		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}[3]	Input LOW Voltage		–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$		110		100	mA
I_{SB1}	Automatic CE Power Down Current —TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}		40		35	mA
I_{SB2}	Automatic CE Power Down Current —CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0		20		20	mA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	12	pF
C_{OUT}	IO Capacitance		12	pF

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	FBGA Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	28.31	51.43	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		11.4	15.8	°C/W

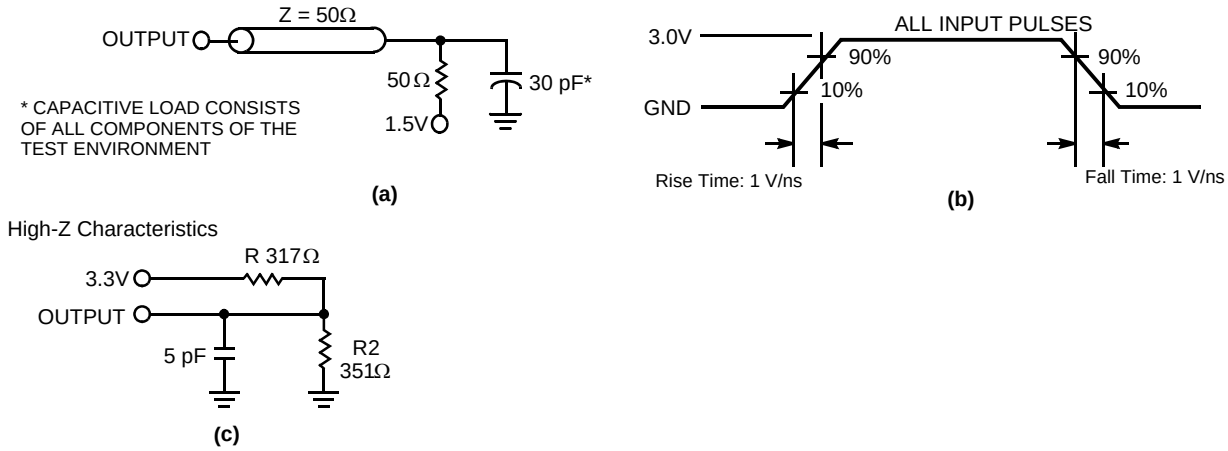
Notes

3. $V_{IL(min)}$ = –2.0V and $V_{IH(max)}$ = V_{CC} + 2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters

AC Test Loads and Waveforms

AC characteristics (except High-Z) are tested using the load conditions shown in Figure 3 (a). High-Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

Figure 3. AC Test Loads and Waveforms

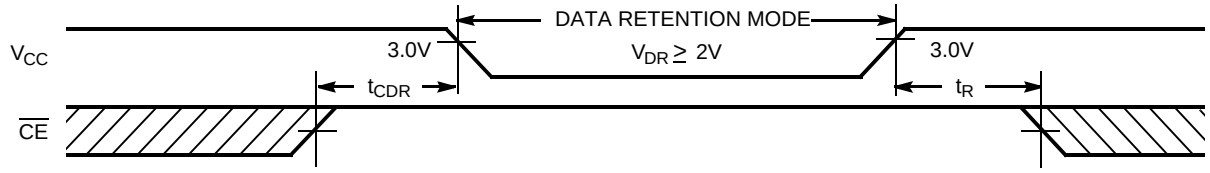


Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions[5]	Min	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		20	mA
t_{CDR}[4]	Chip Deselect to Data Retention Time		0		ns
t_R[6]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform



Notes

5. No inputs may exceed V_{CC} + 0.3V
6. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 50 µs or stable at V_{CC}(min) ≥ 50 µs.

AC Switching Characteristics

Over the Operating Range[7]

Parameter	Description	–10		–12		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}[8]	V_{CC}(typical) to the First Access	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	2.5		2.5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[9, 10]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[10]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[9, 10]		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		6	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		ns
t_{HZBE}	Byte Disable to High-Z		5		6	ns
Write Cycle[11, 12]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		ns
t_{AW}	Address Setup to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Setup to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[10]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[9, 10]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

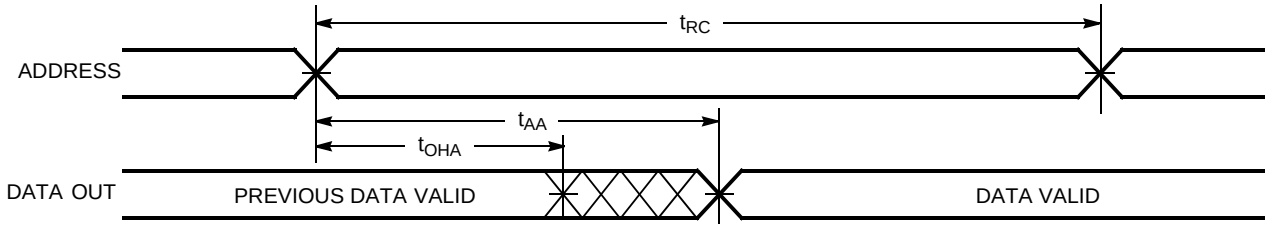
Notes

7. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
8. t_{POWER} gives the minimum amount of time that the power supply must be at typical V_{CC} values until the first memory access can be performed.
9. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of "AC Test Loads and Waveforms" on page 4.Transition is measured when the outputs enter a high impedance state.
10. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any device.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data setup and hold timing must refer to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

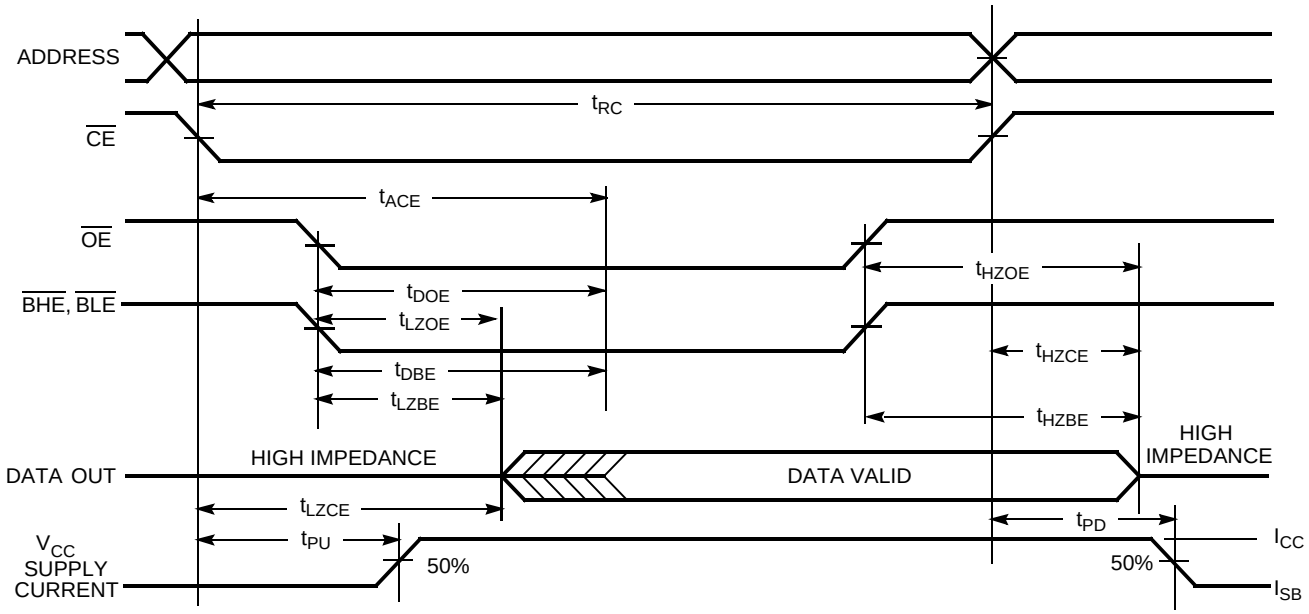
Read Cycle No. 1

Figure 4. Read Cycle No. 1[13, 14]



Read Cycle No. 2 ($\overline{OE}$ Controlled)

Figure 5. Read Cycle No. 2[14, 15]

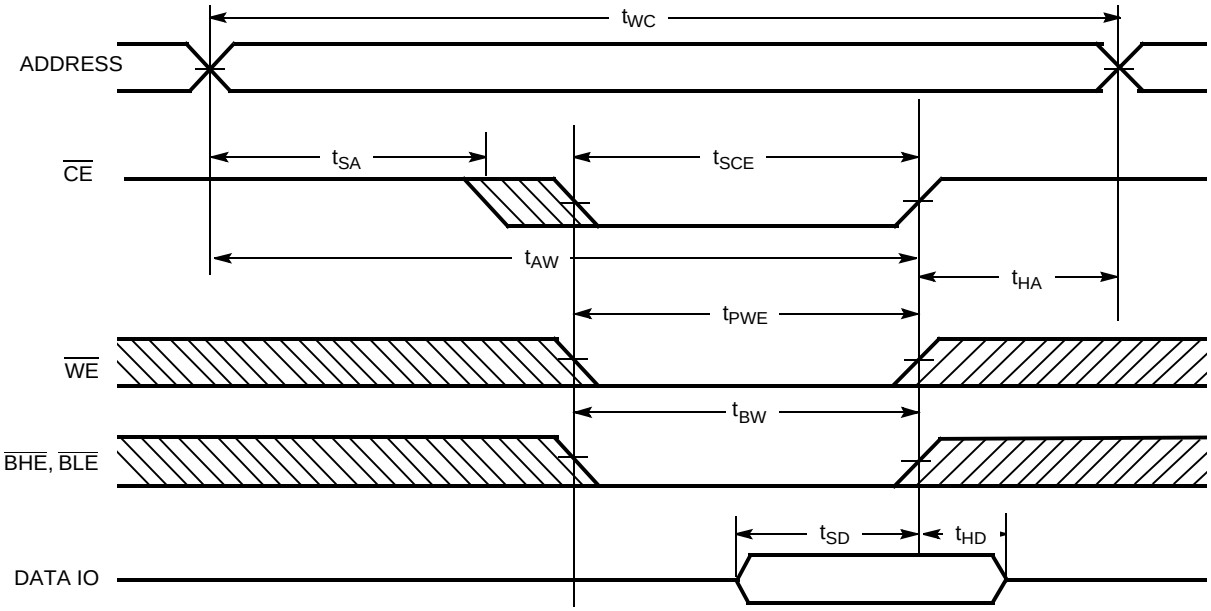


Notes
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
14. $\overline{WE}$ is HIGH for Read cycle.
15. Address valid before or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

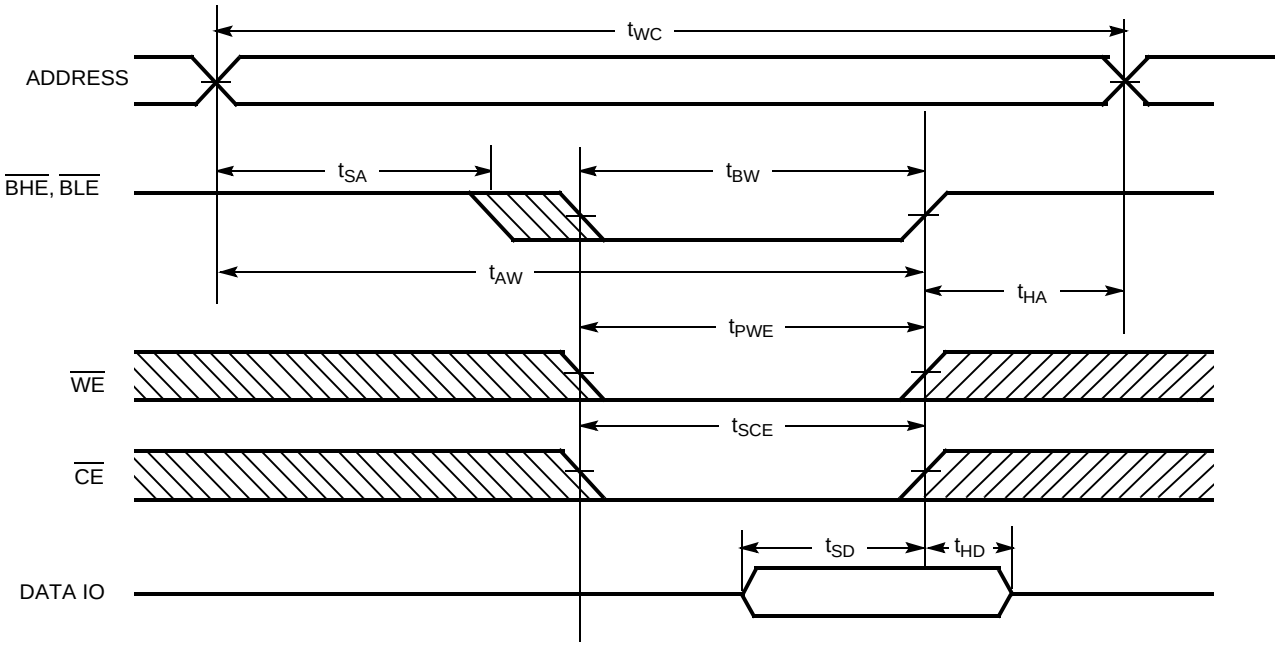
Write Cycle No. 1 ($\overline{CE}$ Controlled)

Figure 6. Write Cycle No. 1[16, 17]



Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

Figure 7. Write Cycle No. 2

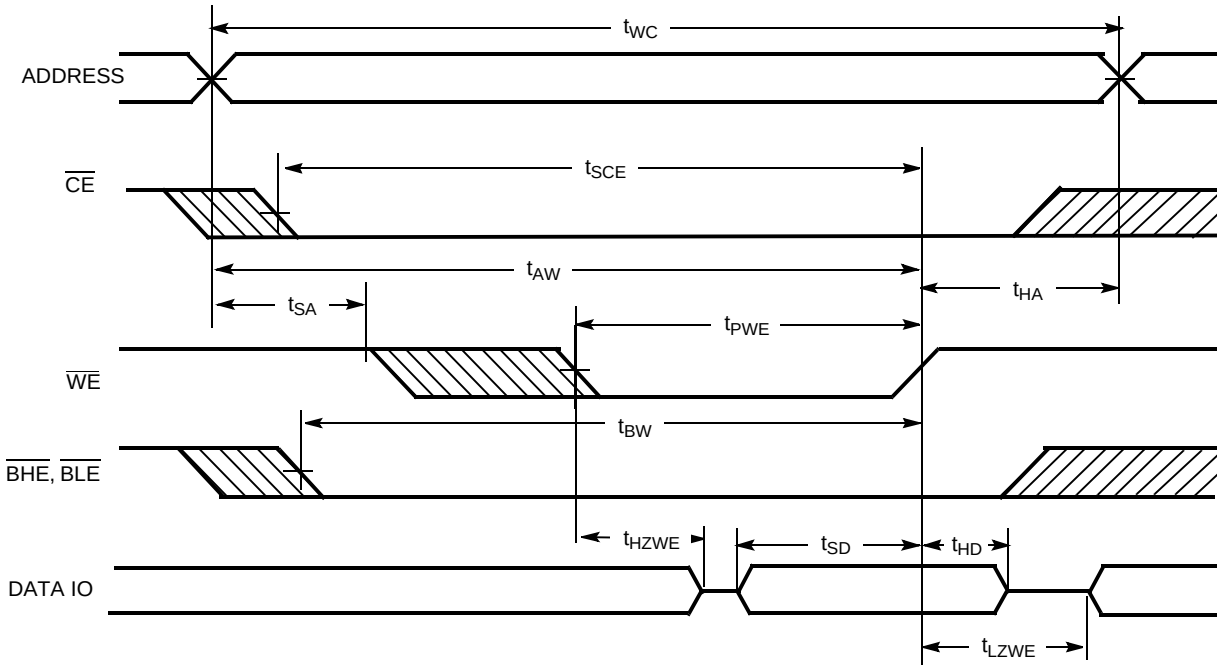


Notes
16. Data IO is high-impedance if $\overline{OE}$, or $\overline{BHE}$, $\overline{BLE}$, or both = V_{IH}.
17. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)

Figure 8. Write Cycle No. 3



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	IO_0–IO_7	IO_8–IO_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

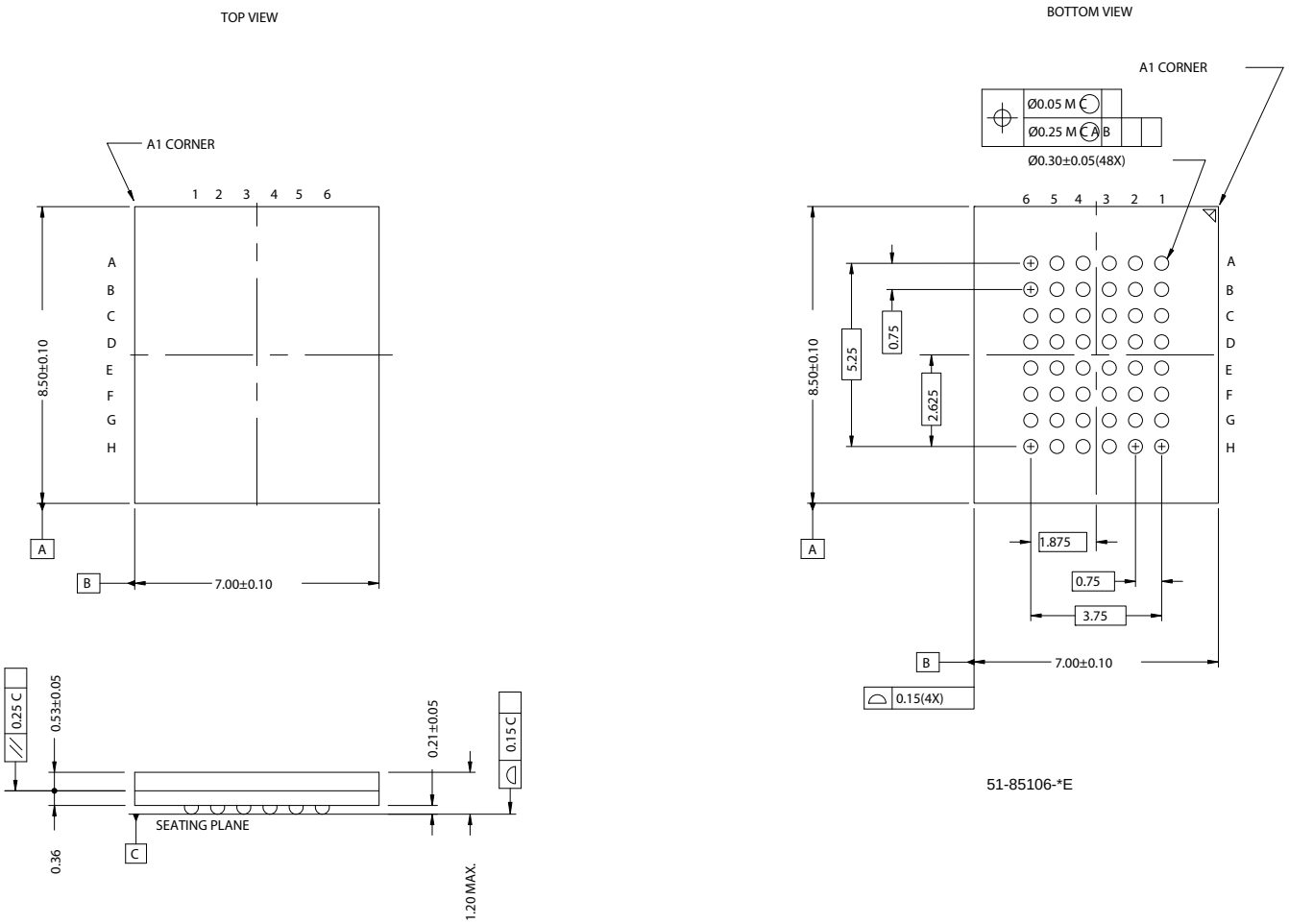
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1051DV33-10BAXI	51-85106	48-ball FBGA (Pb-Free)	Industrial
	CY7C1051DV33-10ZSXI	51-85087	44-pin TSOP II (Pb-Free)	
12	CY7C1051DV33-12BAXI	51-85106	48-ball FBGA (Pb-Free)	
	CY7C1051DV33-12ZSXI	51-85087	44-pin TSOP II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts.

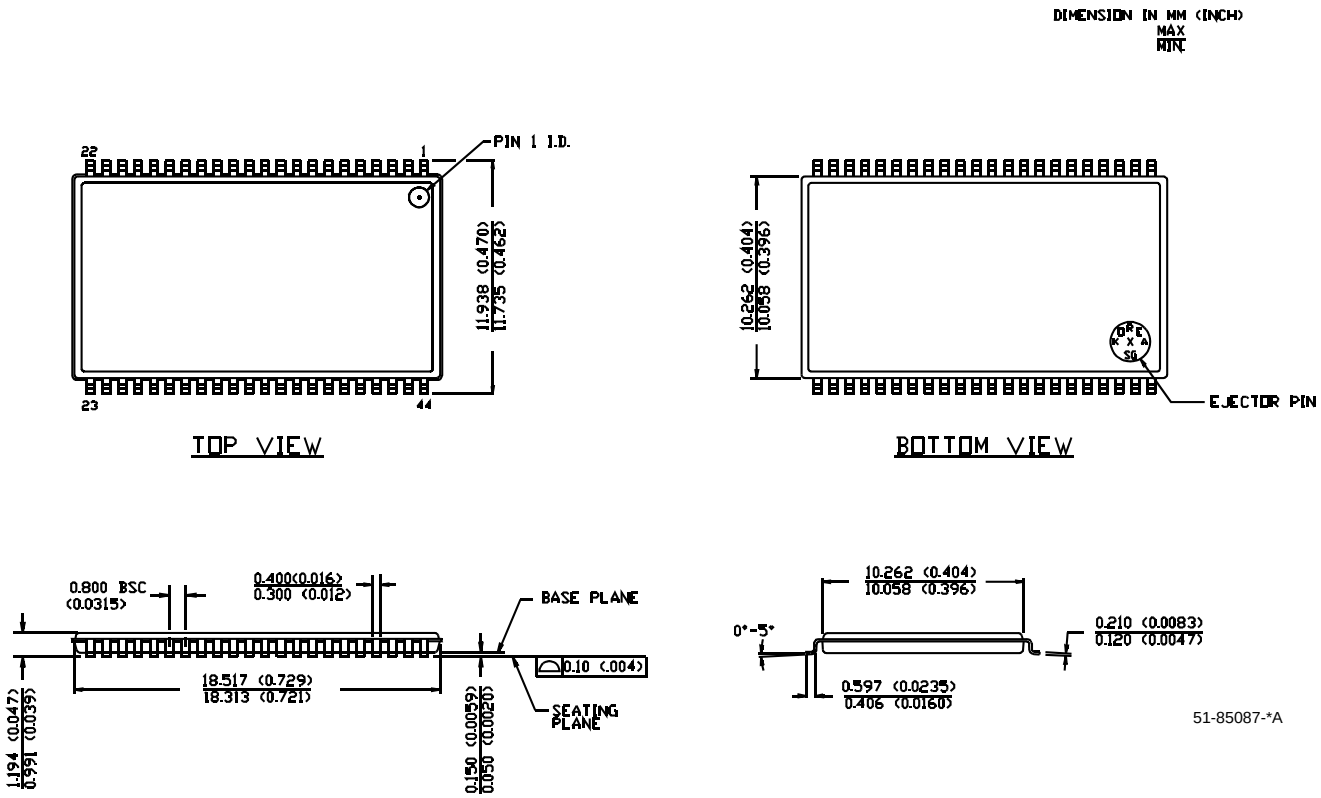
Package Diagrams

Figure 9. 48-Ball FBGA (7.00 mm x 8.5 mm x 1.2 mm) (51-85106)



Package Diagrams (continued)

Figure 10. 44-pin TSOP II (51-85087)



Document History Page

Document Title: CY7C1051DV33, 8-Mbit (512K x 16) Static RAM Document Number: 001-00063				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	342195	See ECN	PCI	New Data Sheet
*A	380574	See ECN	SYT	Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 110, 90 and 80 mA to 110, 100 and 95 mA for 8, 10 and 12 ns speed bins respectively I_{CC} (Ind'l): Changed from 110, 90 and 80 mA to 120, 110 and 105 mA for 8, 10 and 12 ns speed bins respectively Changed the Capacitance values from 8 pF to 10 pF on Page # 3
*B	485796	See ECN	NXR	Changed address of Cypress Semiconductor Corporation on Page# 1 from "3901 North First Street" to "198 Champion Court" Removed -8 and -12 Speed bins from product offering, Removed Commercial Operating Range option, Modified Maximum Ratings for DC input voltage from -0.5V to -0.3V and V_{CC} + 0.5V to V_{CC} + 0.3V Changed the Description of I_{IX} from Input Load Current to Input Leakage Current. Changed t_{HZBE} from 5 ns to 6 ns Updated footnote #7 on High-Z parameter measurement Added footnote #11 Updated the Ordering Information table and Replaced Package Name column with Package Diagram.
*C	866000	See ECN	NXR	Changed ball E3 from V_{SS} to NC in FBGA pin configuration
*D	1513285	See ECN	VKN/AESA	Converted from preliminary to final Changed t_{HZBE} from 6 ns to 5 ns for 10 ns speed bin Added 12 ns speed bin Changed t_{OHA} spec from 3 ns to 2.5 ns Updated Ordering information table